Investigating CMOS Inverters Noise Margins at Different Technologic Nodes

[1]Clayton Farias, [2]Cristina Meinhardt , [1]Paulo F. Butzen
[1]Centro de Ciências Computacionais – C3, Universidade Federal do Rio Grande- FURG
[2]Departamento de Informática e Estatística, Universidade Federal de Santa Catarina - UFSC
{claytonfarias, paulobutzen}@furg.br , cristina.meinhardt@ufsc.br

***Abstract*—This work analyses the Noise Margin of CMOS inverter in four technologic nodes. Two predictive technology models were explored Low Power (LP) and High Performance (HP). The main goal is to explore the behavior of the inverter noise margin with the technology scaling. As expected, the results shows a decrement in noise margin with the technology scaling, mainly due to the supply voltage scaling. When a constant supply voltage is used for the different technology nodes, an increment in the noise margin with the technology scaling is observed.**

Keywords—Inverter;noise margin; nanotechnology.

I. INTRODUCTION

The semiconductor industry is exploring the technology scaling to produce faster integrated circuits at each new technology node. The reduction in transistor dimension has increased the electric field between its structures. The scaling also allows the integration of more devices in the same area, increasing the power consumption per area, and consequently, the heat dissipation. To deal with these drawbacks, the supply voltage has to be reduced.

In advanced technology nodes, the supply voltage is smaller than 1V. This reduced supply voltage let the integrated circuits more susceptible to any noise that can affect the system. For this reason, the noise margin analysis is so relevant in nanometer technology nodes.

In this work, the noise margins of four predictive technologies were explored. These technologies present two transistor models each. The first one is dedicated to high performance design, where the transistors present high saturated current. The second present the transistor with high threshold voltage to design that needs low static power. The paper goal is to investigate the inverter noise margins for these four technology nodes, evaluating the behavior between the noise margins and the technology scaling.

The following Section will discuss the noise margins concepts. Section III presents the methodology used in this work. The simulation results were presented in Section V.

II. NOISE MARGINS

In this Section the basic concepts related to the noise margins are presented. Initially, the high and low noise margins of an inverter are discussed. Later, a method to extract the related values from a DC simulation is present.

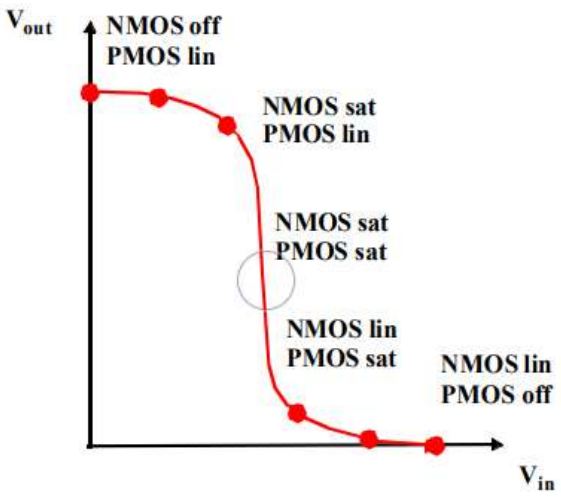

Fig 1. DC transfer curve.

Digital circuits are merely analog circuits used over a special portion of their range. The DC transfer characteristics of a circuit relate the output voltage to the input voltage, assuming the input changes slowly enough that capacitances have plenty of time to charge or discharge. Specific ranges of input and output voltages are defined as valid 0 and 1 logic levels. The DC transfer characteristics of CMOS gates and pass transistors is represent in figure 1 where shows the steps of an inverter in some conditions, showing the transistors NMOS and PMOS in four states:

- Off – The transistor is turn off (not-working)
- On – The transistor is turned on (working)
- Sat – Saturation state
- Lin – Linear state.

Noise margin (NM) is the ability to allow that a noise voltage in an input of a gate does not corrupt the gate output. To evaluate the noise robustness, a DC simulation on CMOS inverter was performed. The resulting curve is show on Fig 1 and 2.

The another curve on figure 2 illustrates the inverter transfer characteristic too however is a quit different than. From this curve was extracted the following parameters:

- VIL – Low Input Voltage
- VOL – Low Output Voltage
- VIH – High Input Voltage
- VOH – High Output Voltage

These logic levels are define at the unity gain point where the slope is –1, as illustrated in Fig. 2. This gives a conservative bound on the worst case off static noise margin [1].

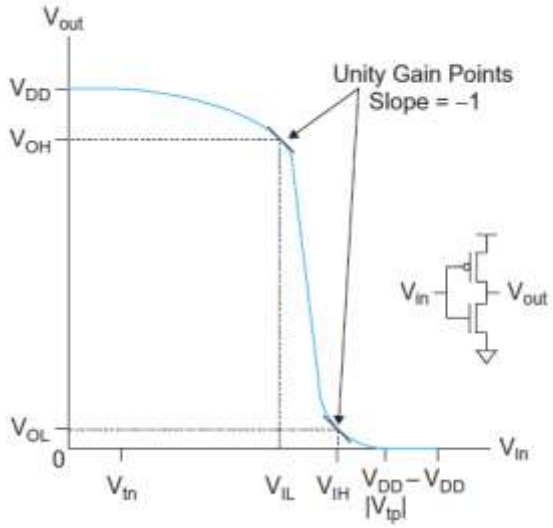

Fig 2.Voltage Transfer Curve of a CMOS inveter [2].

With the previous four parameters computed, it is possible to find the high noise margin (NMH) and low noise Margin (NML). NML is defined by difference in maximum low input voltage (VIL) recognized by receiving gate and the maximum low output voltage (VOL) produced by the driving gate. NMH is the difference in minimum High output voltage (VOH) of driving gate and the minimum High input voltage (VIH) recognized by the receiving gate. Fig. 2 illustrates the described definitions.

The voltage values between VIL and VIH are in the indeterminate region and do not represent legal digital logic levels. Therefore, it is generally desirable to have VIH as close as possible to VIL and for this value to be midway in the logic swing, VOL to VOH. This implies that the transfer characteristic should switch abruptly, that is, there should be high gain in the transition region [2].

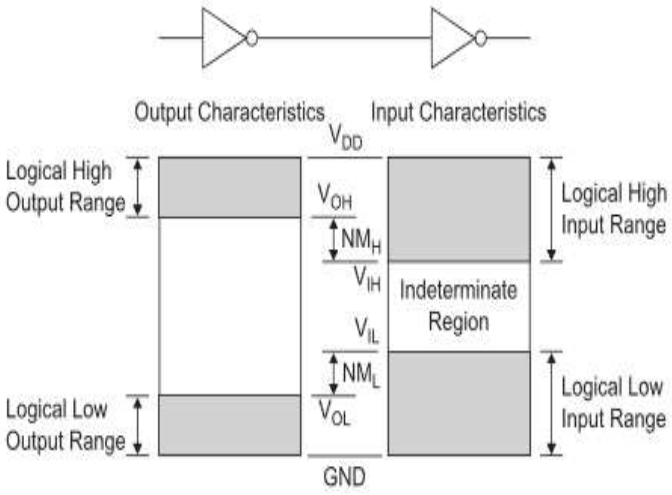

Fig. 3. Noise margin definition from VIL, VOL, VIH, VOH parameters [2].

In case of NML or NMH are too small in a gate, the gate may be disturbed by noise that occurs on the inputs. In case of An unusual gate having equal noise margins, which maximizes immunity to arbitrary noise sources. If a gate sees more noise in the high or low input state, the gate can be changed to improve that noise margin at the expense of the other. Note that the Vtp is the threshold voltage of Pmos transistor and Vtn is the threshold voltage of Nmos transistor. For example, if the module of Vtp is equal to Vtn, then NMH and NML increases as threshold voltages are increased. Quite often, noise margins are compromised to improve the circuit speed.

Noise sources tend to scale together with the supply voltage, so noise margins trade-of as a fraction of the supply voltage. For example, a noise margin of 0.4V is quite stable in a 1.8 V process, but marginal in a 5V supply. DC analysis gives us the static noise margins specifying the level of noise that a gate may see for an indefinite duration. Larger noise pulses may be acceptable if they are brief, these are described as dynamic noise margins specified by [5] a maximum amplitude as a function of the duration. Unfortunately, there is no simple amplitude-duration product that conveniently specifies dynamic noise margins.

III. METHODOLOGY

This section presents the techniques used to find noise margins in this work. Initially, the inverter characteristics, as transistors length and width, for each technology node were presented. Later, details related to the electrical simulation and the noise margins calculations were discussed.

CMOS inverters were designed at the 45nm, 32nm, 22nm and 16nm technologies nodes, in Low Power (LP) and High Performance (HP) technology models provided by PTM [3][4]. The length of all transistor is the size technology node it self. The NMOS width is twice the length and the width of PMOS transistors is twice times the width of NMOS transistors. NGSPICE is the electric simulator used on DC simulation in order to find the transfer curve necessary to calculate noise margins.

The first set of simulations explores the nominal operation conditions. The nominal voltage of each technology model is shown in the third column of Table I. The simulation is performed in room temperature to investigate the noise margins behaviors with the technology scaling.

After, other two sets of simulations were performed. The first explore the minimum supply voltage of LP models. All inverters described using the LP models go to a second round of simulation with a equal voltage of 0.9 V. This is the nominal supply voltage of 16nm LP model, the minimum of all LP models.

The last simulation set uses the smallest supply voltage for all models. The 16nm HP has a nominal supply voltage of 0.7 V. With these two sets of simulations we intend to evaluate the noise margin behavior with the technology scaling without the voltage scaling. With this analysis it is possible verify the real improvement or worsening with the transistor dimension reduction.

IV. RESULTS

This Section is compose in three analysis as presented in the methodology. Table I presents both noise margin NML and NMH in nominal voltage. Almost all noise margins NML demonstrated a lower value than NMH. The exception is the 16nm HP were NML is higher than NMH. In terms of technology scaling, we can confirm the slightly reduction in the noise margins as the technology scales down. This behavior can not be confirmed in NML of 16nm technologies, which shows an improved in the noise margin when compared to the previous technology.

TABLE I. ANALIZE OF NOISE MARGIN IN PTM HP AND LP AT NOMINAL VDD

PTM	Technology	Nominal Voltage	NML	NMH
HP	**45 nm**	1.0	0.48	0.65
	32 nm	0.9	0.46	0.59
	22 nm	0.8	0.44	0.53
	16 nm	0.7	0.45	0.42
LP	**45 nm**	1.1	0.55	0.62
	32 nm	1.0	0.52	0.57
	22 nm	0.95	0.51	0.57
	16 nm	0.9	0.55	0.56

Table II shows the result for LP models with the minimum supply voltage between all LP models. As mention in the methodology this voltage is 0.9 V. Table II also includes one more column when compared to Table I. The Low Rate represents the rate between the smaller noise margins in this case set NML in relation to the supply voltage 0.9V. From the results is possible to observe note that the downsizing of technologies directly impact on an increasing in this low rate.

These info shown that the reduction of sizing in technologic nodes affects directly the noise margins increasing them a little bit conform the technology.

TABLE II. ANALIZE OF NOISE MARGIN IN LP 0.9V

Technology	Model	Voltage (V)	NML	NMH	Low Rate
45nm	**LP**	0.9	0.45	0.51	0.50
32nm	**LP**	0.9	0.47	0.52	0.52
22nm	**LP**	0.9	0.49	0.54	0.54
16nm	**LP**	0.9	0.55	0.56	0.61

Table III shows the result for models with the minimum supply voltage between all models. As mention in the methodology this voltage is 0.7 V. Table III presents the same columns as Table II. The difference between them is the supply voltage and the presence of both technology models. Again, it is possible to observe that as the technology scales down without the supply voltage scaling, the noise margins present a higher value. Also both LP and HP models present similar behavior and values when the worst noise margin is considered. This behavior is very important, since it shows an improved with technology scaling when operating in similar conditions.

TABLE III. ANALIZE OF NOISE MARGIN IN PTM HP AND LP AT 0.7V

PTM	Technology	Voltage(V)	NML	NMH	Low Rate
HP	**45 nm**	0.7	0.34	0.45	0.49
	32 nm	0.7	0.36	0.46	0.51
	22 nm	0.7	0.39	0.46	0.56
	16 nm	0.7	0.45	0.42	0.60
LP	**45 nm**	0.7	0.35	0.40	0.50
	32 nm	0.7	0.36	0.41	0.51
	22 nm	0.7	0.37	0.43	0.53
	16 nm	0.7	0.41	0.44	0.59

V. CONCLUSION

The main goal of this work was observe the behavior of CMOS inverter by using noise margins and comparing the decreasing sizes of these CMOS technologic nodes. Another topic was observe the results generates of tables II and III that shows CMOS inverter has a behavior opposite as the initially expected when downsizing the technology. So, this work shows as the technology continuous downsizing, the noise margins NML and NMH are slightly higher in same operation

conditions, on the same way this occurs with the threshold voltage too.

VI. ACKNOWLEDGMENTS

This article was supported by the FAPERGS organization.

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